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[CHIP PACKAGE STRUCTURE AND PROCESS FOR FABRICATING THE SAME]

Abstract

A chip package structure and a process for fabricating the same is disclosed. The chip package structure mainly comprises a carrier, a chip and an encapsulating material layer. To fabricate the chip package, a carrier and a plurality of chips are provided. Each chip has at least an active surface with a plurality of bumps thereon. The chips and the carrier are electrically connected. An encapsulating material layer that fills the bonding gap between the chips and the carriers and covers the chips and carrier is formed. The encapsulating material layer between the chips and the carrier has a first thickness and the encapsulating material layer over the chips has a second thickness. The second thickness has a value between half to twice the first thickness.